"Greyscale Erosion/Dilation Morphological image processing operators implemented on Hardware FPGA using Xilinx Virtex5 chip"

1. Introduction

Due to the huge data computation needed on majority video processing software applications the engineers and researchers found that the software solutions is less suitable for real-time applications required often for industry, medicine or military defence frameworks. As an alternative existing solutions on the market the final video processing solution can be chose from tree studied possibility: using predefined DSP processor, using four 3 GHz INTEL XEON multiprocessor structure or with the new FPGA (Field Programmable Gate Array) support. Estimated result for FPGA implementation is between 25-100 ms whereas for DSP and multiprocessor system is 3, 5 s and 2 seconds respectively. On the vertical axis the estimated price in euro for these tree systems is represented. From the graph we conclude that the new FPGA solution meet the real-time requirement assuming that we need approximately 30 ms to process one 640*480 frame.

![Graph](image)

**Graph1.FPGA, DSP and multiprocessor system time estimation**

2. Task implementation

Morphological operations are very intensive used today to extract regional features and shape information from images within pattern recognition or image understanding tasks. So the aim of this master project is to implement basic morphological dilation/erosion, on hardware. The board and the software tools used for this work will be the package provided by Xilinx Company which consists on ML 505 board and ISE 9.2i and EDK 9.2i software [1]. In order to implement one dilation /erosion hardware module on FPGA hardware first the morphological dilation/erosion concept must be defined. To implement the FPGA approach, the solution is to move the input image not SE in such way that the image is centred on a new pixel at each clock pixel and with a rate with one pixel per clock.[2]Therefore, the keep in mind operations to build such module will be:

1. Compare pixels within a neighbourhood covered by SE
2. Replace the central pixels with the result of the erosion/dilatation operations
3. Shifting the input image or SE
4. Repeat the tree previous operations
Regarding the FPGA implementation of this erosion/dilation module there several methods exist. You may choose to write HDL specification by your self [3] or you may chose to build the synthesisable gate-level module using ISE 9.2i Xilinx software tool [2]. Because we deal with grayscale images application which have a range of pixels intensity values from 0 to 255 we must consider that the hardware implementation using FPGA is much more complicated. These are not simple tasks because the generally FPGA based operations are based on simple bit operations (not bytes); therefore all the byte-operations will be customized and tested for our further morphological image application.

Bibliography:


*ISE DOCUMENTATION:* http://www.xilinx.com/ise/logic_design_prod/foundation.htm

*EDK DOCUMENTATION:* http://www.xilinx.com/ise/embedded_design_prod/platform_studio.htm

[2]. Development of Morphological Operators for Field Programmable Gate Arrays - A J Tickle, J S Smith, Q H Wu, Department of Electrical Engineering and Electronics, The University of Liverpool, Liverpool L69 3GJ, U.K. (or Erosion and dilation model test circuit .PDF)


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